信昌電子陶瓷股份有限公司
Prosperity Dielectrics Co., Ltd.

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Messrs.：____

Date：___

APPROVAL SHEET

Product Name ：Stacked Capacitors

Part No. ：FE Series

Description ：Size 1210~2225, C0G/X7R, 50Vdc to 1000Vdc

PREPARED BY	APPROVED BY

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SPECIFICATION

FOR

Product Name ： **Stacked Capacitors**

Part No. ： **FE Series**

Description ： **Size 1210~2225, C0G/X7R, 50Vdc to 1000Vdc**

SPEC. No.	：**FE-000-001-03**
DATE	：

DRAWN BY	CHECEKED BY	APPROVED BY
Yvens Chou	**Yvens Chou**	**Ryan Chen**

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1. INTRODUCTION

FE Series green type capacitors are manufactured by using green materials without lead and cadmium. These capacitors to achieve a unique structure of high reliability. The use of metal lead frame, can absorb the heat and mechanical stress. ESR (equivalent series resistance), ESL (equivalent series inductance) is small, the most suitable for high frequency operation of the rectifier power supply.

2. FEATURES

a. High reliability and stability.
b. Higher mechanical endurance.
c. Anti thermal stress and mechanical stress.
d. Improved vibration performance.
e. More capacitance without changing footprint.
f. RoHS Compliant.

3. APPLICATIONS

a. DC to DC converter.
b. High voltage coupling/DC blocking.
c. Back-lighting inverters.
d. Snubbers in high frequency power converters.
e. Power supplies.
f. Surge protection.
g. Filtering, smoothing, and decoupling application.

4. HOW TO ORDER

FE	2H	X	105	K	631	E	D	L
PDC Family	Chip q'ty and size	Dielectric	Capacitance	Tolerance	Rated Voltage	Packaging	Thickness	Control Code
Table1	Table2	Table3	Table4	Table5	Table6	Table7	Table8	Table9

Table 1 PDC family

Code	Description
FE	Stacked Capacitors Series

Table 2 Stack chip quantity and chip size

The first digit : # of chips in stack

Second digit code : chip size (below)

Code	Description	Code	Description	Code	Description
A	1210 (3225)	G	1825 (4563)	I	2225 (5763)
C	1812 (4532)	H	2220 (5750)		

Table 3 Dielectric Material Characteristics

Code	Description	Code	Description
N	C0G	X	X7R

Table 4 Table 4 Capacitance Rule Code

Code	Description	Code	Description
R47	0.47pF	102	$102=10x10^{2}=1000pF$
0R5	0.5pF	104	$104=10x10^{4}=100nF$
100	$100=10x10^{0}=10pF$	106	$106=10x10^{6}=10\mu F$

Table 5 Tolerance

Code	Description	Code	Description	Code	Description
A	±0.05 pF	I	-10% ~ 0%	Q	±0.03 pF
B	±0.10 pF	J	±5 %	Z	-20% ~ +80%
C	±0.25 pF	K	±10 %	X	+10% ~+20%
D	±0.50 pF	L	0% ~ +10%		
F	±1 %	M	±20 %		
G	±2 %	N	-5% ~ +10%		
H	±3 %	P	±0.02 pF		

Table 6 Rated voltage

Code	Description	Code	Description	Code	Description
500	50Vdc	251	250Vdc	102	1000Vdc
101	100Vdc	501	500Vdc		
201	200Vdc	631	630Vdc		

Table 7 Packaging Type

Code	Description	Code	Description
B	Bulk	E	Tape and 7" Reel, Embossed Tape
T	Tray package	L	Tape and 13" Reel, Embossed Tape

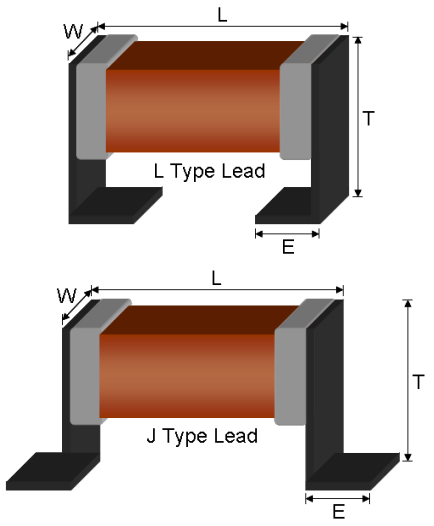
Table 8 Thickness Description

Code	Description	Code	Description	Code	Description
A	3.00±0.30 mm	J	7.80±0.30 mm	S	12.60±0.30 mm
B	3.60±0.30 mm	K	8.40±0.30 mm	T	13.20±0.30 mm
C	4.20±0.30 mm	L	9.00±0.30 mm		
D	4.80±0.30 mm	M	9.60±0.30 mm		
E	5.40±0.30 mm	N	10.20±0.30 mm		
F	6.00±0.30 mm	P	10.80±0.30 mm		
G	6.60±0.30 mm	Q	11.40±0.30 mm		
H	7.20±0.30 mm	R	12.00±0.30 mm		

Table 9 Special Control Code

Code	Description
L	L type lead
J	J type lead
S	Straight type lead

5. EXTERNAL DIMENSIONS

Size Inch (mm)	L (mm)	W (mm)	T (mm)	E (mm)	
1210 (3225)	3.50±0.40	2.50±0.40	Reference Table 8	1.70±0.15	
1812 (4532)	4.80±0.40	3.20±0.40		1.70±0.15	
1825 (4563)	4.80±0.40	6.30±0.50		1.70±0.15	
2220 (5750)	6.00±0.40	5.00±0.50		1.70±0.15	
2225 (5763)	6.00±0.40	6.30±0.50		1.70±0.15	Fig.5-1 The outline of Stacked Capacitors

6. GENERAL ELECTRICAL DATA

<table>
<tr><td>Dielectric</td><td>C0G</td><td>X7R</td></tr>
<tr><td>Size</td><td>1210, 1812, 1825, 2220, 2225</td><td>1210, 1812, 1825, 2220, 2225</td></tr>
<tr><td>Rated voltage (WVDC)</td><td>50V, 100V, 200V, 250V, 500V, 630V, 1000V</td><td>50V, 100V, 200V, 250V, 500V, 630V, 1000V</td></tr>
<tr><td>Capacitance range*</td><td>660nF Max.</td><td>44µF Max.</td></tr>
<tr><td>Capacitance tolerance</td><td>Reference to Table5</td><td>Reference to Table5</td></tr>
<tr><td>Tan δ</td><td><table><tr><th>Cap. Range</th><th>Q Spec.</th></tr><tr><td>Cap<30pF:</td><td>Q≥400+20C</td></tr><tr><td>Cap≥30pF:</td><td>Q≥1000</td></tr></table></td><td>For 1 chip in stack≤2.5%
For 2 chips in stack≤5.0%</td></tr>
<tr><td rowspan="3">Capacitance & Tan δ Test condition</td><td>Measured at the condition of 30~70% related humidity</td><td>Measured at the condition of 30~70% related humidity</td></tr>
<tr><td>For 25℃ at ambient temperature</td><td>Preconditioning for Class II MLCC : Perform a heat treatment at 150±10℃ for 1 hour, then leave in ambient condition (25℃) for 24±2 hours before measurement</td></tr>
<tr><td><table><tr><th>Cap. Range</th><th>Test Condition</th></tr><tr><td>Cap.≤1000pF</td><td>1.0±0.2Vrms, 1.0MHz±10%</td></tr><tr><td>Cap.>1000pF</td><td>1.0±0.2Vrms, 1.0KHz±10%</td></tr></table></td><td><table><tr><th>Cap. Range</th><th>Test Condition</th></tr><tr><td>Cap.≤10µF</td><td>1.0±0.2Vrms, 1.0KHz±10%</td></tr><tr><td>Cap.>10µF</td><td>0.5±0.2Vrms, 120KHz±20%</td></tr></table></td></tr>
<tr><td>Insulation resistance at Ur</td><td>≥100GΩ or RxC≥500Ω-F,
whichever is smaller</td><td>≥10GΩ or RxC≥100Ω-F,
whichever is smaller</td></tr>
<tr><td>Operating temperature</td><td>-55 to +125℃</td><td>-55 to +125℃</td></tr>
<tr><td>Capacitance characteristic</td><td>±30ppm / ℃</td><td>±15%</td></tr>
<tr><td>Lead frame</td><td>L / J / Straight type lead</td><td>L / J / Straight type lead</td></tr>
</table>

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7. CAPACITANCE RANGE (Max.)

7-1. C0G

Dimension	Code	Rated Voltage						
		50V	100V	200V	250V	500V	630V	1000V
1210	1A	683	473	333	333	183	153	392
	2A	134	104	663	663	363	333(M)	782
1812	1C	154	104	563	563	393	333	562
	2C	334(M)	224(M)	124	124	783	663	123
1825	1G	154	124	104	104	683	683	123
	2G	334(M)	244	204	224(M)	134	134	243
2220	1H	274	184	104	104	683	563	123
	2H	544	364	224(M)	224(M)	134	124	243
2225	1I	334	224	154	154	104	823	123
	2I	664	444	334(M)	334(M)	224(M)	164	243

7-2. X7R

Dimension	Code	Rated Voltage						
		50V	100V	200V	250V	500V	630V	1000V
1210	1A	475	335	684	684	154	154	683
	2A	106	665	135	135	334(M)	334(M)	134
1812	1C	106	565	105	105	474	184	104
	2C	226(M)	126	225(M)	225(M)	105	364	224(M)
1825	1G	106	106	275	275	824	824	334
	2G	226(M)	226(M)	545	545	165	165	664
2220	1H	226	106	275	275	105	105	394
	2H	446	226(M)	545	545	225(M)	225(M)	784
2225	1I	226	106	395	395	155	155	394
	2I	446	226(M)	785	785	335(M)	335(M)	784

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8. RELIABILITY TEST CONDITIONS AND REQUIREMENTS

<table>
<tr><th>No.</th><th>Item</th><th>Test Condition</th><th>Requirements</th></tr>
<tr><td>1.</td><td>Visual and Dimensions</td><td>---</td><td>* No remarkable defect.
* Dimensions to confirm to individual specification sheet.</td></tr>
<tr><td>2.</td><td>Capacitance</td><td></td><td>* Shall not exceed the limits given in the detailed spec.</td></tr>
<tr><td>3.</td><td>Q/D.F. (Dissipation Factor)</td><td>* Class I :
Cap.≤1000pF, 1.0±0.2Vrms, 1MHz±10%.
Cap.>1000pF, 1.0±0.2Vrms, 1KHz±10%.
* Class II :
Cap.≤10μF, 1.0±0.2Vrms, 1KHz±10%.
Cap.>10μF, 0.5±0.2Vrms, 120Hz±20%.</td><td>
<table>
<tr><th>Dielectric</th><th>Rated vol.(V)</th><th>Q/D.F.</th><th>Remark</th></tr>
<tr><td rowspan="2">Class I (C0G)</td><td rowspan="2">All</td><td>Q≥1000</td><td>Cap.≥30pF</td></tr>
<tr><td>Q≥400+20C</td><td>Cap.<30pF</td></tr>
<tr><td rowspan="2">Class II (X7R)</td><td>1 chip in stack</td><td>D.F.≤2.5%</td><td>---</td></tr>
<tr><td>2 chips in stack</td><td>D.F.≤5.0%</td><td>---</td></tr>
</table>
</td></tr>
<tr><td>4.</td><td>Temperature Coefficient</td><td>* With no electrical load.
<table>
<tr><th>T.C.</th><th>Operating Temp</th></tr>
<tr><td>C0G</td><td>-55~125℃ at 25℃</td></tr>
<tr><td>X7R</td><td>-55~125℃ at 25℃</td></tr>
</table>
</td><td>
<table>
<tr><th>T.C.</th><th>Capacitance Change</th></tr>
<tr><td>C0G</td><td>Within ±30ppm/℃</td></tr>
<tr><td>X7R</td><td>Within ±15%</td></tr>
</table>
</td></tr>
<tr><td>5.</td><td>Insulation Resistance</td><td>
<table>
<tr><th>Rated vol.(V)</th><th>Apply Voltage</th><th>Test Condition</th></tr>
<tr><td>=100</td><td>1 times of U_R</td><td>Max. 120 sec.</td></tr>
<tr><td>100<V≤500</td><td>1 times of U_R</td><td>60 sec.</td></tr>
<tr><td>>500</td><td>500VDC</td><td>60 sec.</td></tr>
</table>
</td><td>
<table>
<tr><th>Dielectric</th><th>Requirements</th></tr>
<tr><td>Class I</td><td>≥100GΩ or RxC≥500Ω-F, whichever is smaller</td></tr>
<tr><td>Class II</td><td>≥10GΩ or RxC≥100Ω-F, whichever is smaller</td></tr>
</table>
</td></tr>
<tr><td>6.</td><td>Dielectric Strength</td><td>
<table>
<tr><th>Rated vol.(V)</th><th>Condition</th></tr>
<tr><td>≤250</td><td>2 times of U_R</td></tr>
<tr><td>250<V≤500</td><td>1.5 times of U_R</td></tr>
<tr><td>630≤V≤1000V</td><td>1.2 times of U_R</td></tr>
</table>
* Duration : 1 to 5 sec.
* Charge and discharge current less than 50mA.</td><td>* No evidence of damage or flashover during test.</td></tr>
<tr><td>7.</td><td>Temperature Cycle</td><td>* Conduct the 100 cycles according to the temperatures and time.
<table>
<tr><th>Step</th><th>Temp.(℃)</th><th>Time(min.)</th></tr>
<tr><td>1</td><td>Min. operating temp. +0/-3</td><td>30±3</td></tr>
<tr><td>2</td><td>Room temp.</td><td>2~3</td></tr>
<tr><td>3</td><td>Max. operating temp. +3/-0</td><td>30±3</td></tr>
<tr><td>4</td><td>Room temp.</td><td>2~3</td></tr>
</table>
* Before initial measurement (Class II only) : Perform 150+0/-10℃ for 1 hr and then set for 48±4 hrs at room temp.
* Measurement to be made after keeping at room temp. for 24±2 hrs (Class I) or 48±4 hrs (Class II).</td><td>* No remarkable damage.
<table>
<tr><th>Dielectric</th><th>I.R.</th><th>Cap. Change</th><th>Q/D.F.</th></tr>
<tr><td>Class I (C0G)</td><td rowspan="2">To meet initial requirement</td><td>Within ±2.5% or ±0.25pF, whichever is larger</td><td>≤1.0(Q) × initial requirement</td></tr>
<tr><td>Class II (X7R)</td><td>Within ±7.5%</td><td>≤1.5(D.F.) × initial requirement</td></tr>
</table>
</td></tr>
<tr><td>8.</td><td>Humidity (Damp Heat) Steady State</td><td>* Test temp. : 40±2℃.
* Humidity : 90~95%RH.
* Test time : 500 +24/-0 hrs.
* Measurement to be made after keeping at room temp. for 24±2 hrs (Class I) or 48±4 hrs (Class II).</td><td>* No remarkable damage.
<table>
<tr><th>Dielectric</th><th>I.R.</th><th>Cap. Change</th><th colspan="2">Q/D.F.</th></tr>
<tr><td rowspan="3">Class I (C0G)</td><td rowspan="3">≥1G or RxC≥ 50Ω-F, whichever is smaller</td><td rowspan="3">Within ±5.0% or ± 0.5pF, whichever is larger</td><td>Cap.≥30pF</td><td>Q≥350</td></tr>
<tr><td>10pF≤Cap.< 30pF</td><td>Q≥275+2.5C</td></tr>
<tr><td>Cap.<10pF</td><td>Q≥200+10C</td></tr>
<tr><td>Class II (X7R)</td><td>Within ±12.5%</td><td colspan="2">D.F.≤200% of initial requirement</td></tr>
</table>
</td></tr>
</table>

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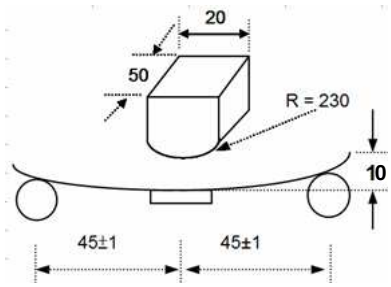
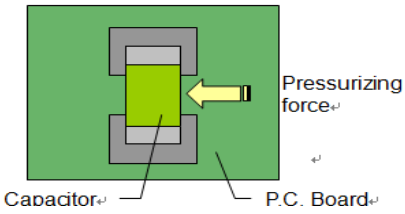
8. RELIABILITY TEST CONDITIONS AND REQUIREMENTS

<table>
<tr><th>No.</th><th>Item</th><th>Test Condition</th><th>Requirements</th></tr>
<tr><td>9.</td><td>Humidity (Damp Heat) Load</td><td>* Test temp. : 40±2℃.
* Humidity : 90~95% RH.
* Test time : 500 +24/-0hrs.
* To apply voltage : Rated voltage (Max. 500Vdc).
* Measurement to be made after keeping at room temp. for 24±2 hrs (Class I) or 48±4 hrs (Class II).</td><td>* No remarkable damage.
<table>
<tr><th>Dielectric</th><th>I.R.</th><th>Cap. Change</th><th colspan="2">Q/D.F.</th></tr>
<tr><td rowspan="3">Class I (C0G)</td><td rowspan="4">≥1GΩ or RxC≥ 50Ω-F, whichever is smaller</td><td rowspan="3">Within ±7.5% or ±0.75pF, whichever is larger</td><td>Cap.≥30pF</td><td>Q≥350</td></tr>
<tr><td>10pF≤Cap. <30pF</td><td>Q≥275+2.5C</td></tr>
<tr><td>Cap.<10pF</td><td>Q≥200+10C</td></tr>
<tr><td>Class II (X7R)</td><td>Within ±12.5%</td><td colspan="2">D.F.≤200% of initial requirement</td></tr>
</table></td></tr>
<tr><td>10.</td><td>High Temperature Load (Endurance)</td><td>* Test temp. : 125±3℃.
<table>
<tr><th>Dielectric</th><th>Rated Vol.(V)</th><th>Apply Voltage</th></tr>
<tr><td rowspan="4">C0G/X7R</td><td>≤250</td><td>2.0 times of U_R</td></tr>
<tr><td>250<V≤ 500</td><td>1.5 times of U_R</td></tr>
<tr><td>=630</td><td>1.2 times of U_R</td></tr>
<tr><td>=1000</td><td>1.1 times of U_R</td></tr>
</table>
* Exception items (X7R only) :
<table>
<tr><th>Rated Vol.(V)</th><th>Size</th><th>Cap. Range (Single chip)</th><th>Apply Voltage</th></tr>
<tr><td rowspan="7">50 & 100</td><td>0805</td><td>≥124</td><td rowspan="10">1.5 times of U_R</td></tr>
<tr><td>1206
1210
1812
1825
2220
2225</td><td>≥105</td></tr>
<tr><td rowspan="3">200 & 250</td><td>1210</td><td>>224</td></tr>
<tr><td>1812</td><td>>474</td></tr>
<tr><td>1825
2220
2225</td><td>≥105</td></tr>
</table>
* Test time : 1000 +24/-0 hrs.
* Measurement to be made after keeping at room temp. for 24±2 hrs (Class I) or 48±4 hrs (Class II).</td><td>* No remarkable damage.
<table>
<tr><th>Dielectric</th><th>I.R.</th><th>Cap. Change</th><th>Q/D.F.</th></tr>
<tr><td>Class I (C0G)</td><td rowspan="2">≥1GΩ or RxC≥50 Ω-F, whichever is smaller</td><td>Within ± 3.0% or ± 0.3pF, whichever is larger</td><td rowspan="2">D.F.≤200% of initial requirement</td></tr>
<tr><td>Class II (X7R)</td><td>Within ±12.5%</td></tr>
</table></td></tr>
<tr><td>11.</td><td>Resistance to Flexure of Substrate</td><td>* The middle part of substrate shall be pressurized by means of the pressurizing rod at a rate of about 1mm per second until the deflection becomes 10mm.
 

Unit : mm</td><td>* No remarkable damage.
<table>
<tr><th>Dielectric</th><th>Cap. Change</th></tr>
<tr><td>Class I (C0G)</td><td>Within ±3.0% or ±0.3pF, whichever is larger</td></tr>
<tr><td>Class II (X7R)</td><td>Within ±12.5%</td></tr>
</table>
(This capacitance change means the change of capacitance under specified flexure of substrate from the capacitance measured before the test)</td></tr>
</table>

8. RELIABILITY TEST CONDITIONS AND REQUIREMENTS

No.	Item	Test Condition	Requirements
12.	**Adhesive Strength of Termination**	* Capacitors mounted on a substrate. A force of 10N applied perpendicular to the place of substrate and parallel the line joining the center of terminations for 10±1 second.  	* No remarkable damage or removal of the terminations.
13.	**Vibration Resistance**	* Vibration frequency : 10~55 Hz/min. * Total amplitude : 1.5mm. * Test time : 6 hrs. (Two hours each in three mutually perpendicular directions)	* No remarkable damage. * Cap. change and Q/D.F. : To meet initial spec.

9. APPLICATION NOTES

STORAGE

To prevent the damage of solderability of terminations, the following storage conditions are recommended :

Indoors under 5 ~ 40℃ and 20% ~ 70% RH.

No harmful gases containing sulfuric acid, ammonia, hydrogen sulfide or chlorine.

Packaging should not be opened until the capacitors are required for use. If opened, the pack should be re-sealed as soon as is practicable. Taped product should be stored out of direct sunlight, which might promote deterioration in tape or adhesion performance. The product is recommended to be used within 12 months after shipment and checked the solderability before use.

HANDLING

Chip capacitors are dense, hard, brittle, and abrasive materials. They are liable to suffer mechanical damage, in the form of cracks or chips. Chip Capacitors should be handled with care to avoid contamination or damage. To use vacuum or plastic tweezers to pick up or plastic tweezers is recommended for manual placement. Tape and reeled packages are suitable for automatic pick and placement machine.

PREHEAT

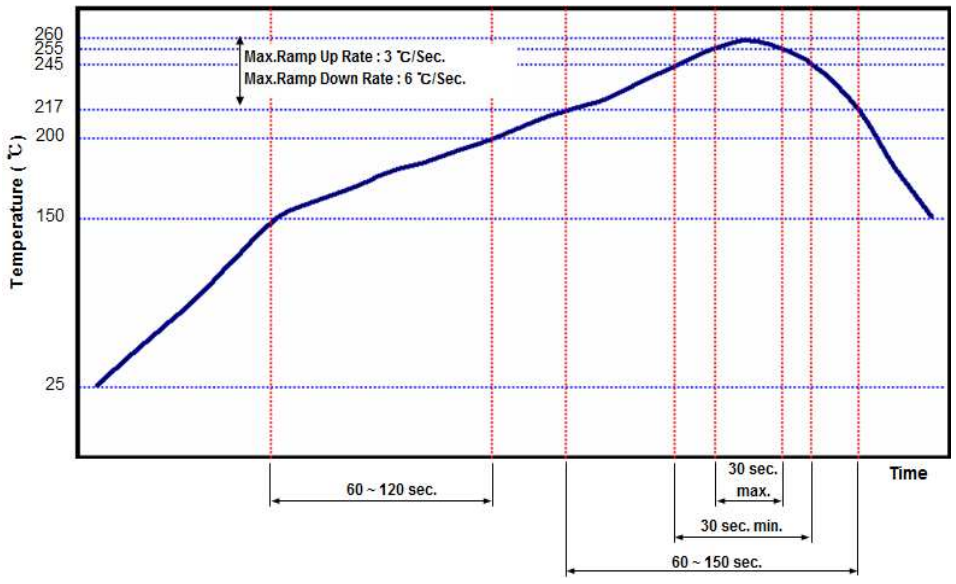
In order to minimize the risk of thermal shock during soldering, a carefully controlled preheat is required. The rate of preheat should not exceed 3℃ per secon d.

SOLDERING

Use middy activated rosin RA and RMA fluxes do not use activated flux. The amount of solder in each solder joint should be controlled to prevent the damage of chip capacitors caused by the stress between solder, chips, and substrate.

a.) Reflow soldering :

Fig.9.1 Reflow soldering profile



For Sn/Ag/Cu Series solder paste (Pb-Free)

COOLING

After soldering, cool the chips and the substrate gradually to room temperature. Natural cooling in air is recommended to minimize stress in the solder joint.

9. APPLICATION NOTES

CLEANING

All flux residues must be removed by using suitable electronic-grade vapor-cleaning solvents to eliminate contamination that could cause electrolytic surface corrosion. Good results can be obtained by using ultrasonic cleaning of the solvent. The choice of the proper system is depends upon many factors such as component mix, flux, and solder paste and assembly method. The ability of the cleaning system to remove flux residues and contamination from under the chips is very important.